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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 22

Application Number: 09/685,362
Filing Date: October 10, 2000
Appellant(s): HUBNER ET AL.

Alfred K. Dassler
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 10, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-4 and 6-9 do stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,563,762	Leung et al.	10-1996
5,972,788	Ryan et al.	10-1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan et al. (US 5,972,788) in view of Leung et al. (US 5,563,762).

Ryan et al. shows (figs. 1-3) semiconductor component comprising a first metal layer (M1) forming a first metal area (21) and a second metal area (24) electrically isolated from each other. A dielectric layer (16) is formed over the first metal area. A second metal layer (M2) forms a third metal area (22) insulated from the first metal layer by an interposition of said dielectric layer (16), the second metal layer together with the dielectric layer and the first metal area form a memory element (capacitor). The second metal layer (M2) further forms a fourth metal area (25) which together with the second metal area (24) forms a contact area to make contact with the second metal layer (metal 34 connects metal layers 25 and 24 together). An additional insulating layer (31) is formed over a contact (25 and 24). An opening is formed in the insulating layer and is filled with conductive material (34) to form an external connection to the contact area. The fourth metal area (25) is separated from the second metal area (24) by interposition of the dielectric layer (16). One further opening (33) is formed in the insulation layer. With respect to the limitations of claim 2, the contact area of combined cited references inherently forms an etching resist because it has the same structure and materials as the instant invention. Ryan et al. shows all of the elements of the claims except the fourth metal area making direct contact with the second metal area, the second metal layer having a connection between the third and fourth metal area, and the various materials used to form the metal and dielectric layers. Leung et al. shows (fig. 3) a semiconductor component having a capacitor structure (128, 130, and 134) and a contact area having a fourth metal area (134) in direct contact with a second metal area (126). The capacitor has an electrically conductive connection between the third metal

area (134) of the capacitor and the fourth metal area of the contact structure (134) because each area is formed simultaneously by the second layer (134). With this configuration, interconnection is made simultaneously with the capacitor top electrode and the contact area to underlying metallization without disrupting routing of the underlying interconnect (col. 8, lines 30-48). The first and second metal layers are composed of a noble metal including platinum and the dielectric is composed of a ferroelectric (col. 11, line 43-col. 12, line 4). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the capacitor and contact structure of Ryan by forming the connection between the capacitor top electrode and contact portion simultaneously as taught by Leung to simplify the interconnection process and form a capacitor structure above the semiconductor without disrupting routing of the underlying interconnect metallization.

With respect to the etching process of claim 2, a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15** at 17(footnote 3). See also in re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon

the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

(11) Response to Argument

The appellant primarily argues that (1) the capacitor of Ryan et al. is an analog capacitor, therefore not forming a memory element and that (2) the combination of Ryan and Leung do not lead to the claimed invention. The examiner believes that the capacitor of Ryan is a memory element based on the reading of the limitations of the appellant's claimed invention and that the combination of Ryan and Leung show all of the elements of the claims because each reference is analogous art.

(1) The appellant argues that the capacitor of Ryan et al. is not a memory element because the capacitor is analog. The appellant then cites column 3, lines 6-17 of Ryan to show that the capacitor is analog. Upon reading of those lines, Ryan does not specifically state that the capacitor of the invention is used for analog or digital devices but discloses the general state of the art concerning capacitors. The lines recite broad information concerning digital and analog devices and mention that trench capacitors save space in large dynamic memories. In essence, column 3 briefly mentions the well known use of capacitors in analog and digital (memory) circuits. Therefore one of

ordinary skill in the art would assume that the invention of Ryan is applicable in analog and digital elements. Furthermore, the structure of a capacitor in an analog device and memory device is generally the same; each comprise a dielectric between two conductor plates.

The appellant's arguments pertaining to the capacitor of Ryan not being a memory element are however irrelevant. Claim 1 of the instant invention specifically states that "said third metal area together with said dielectric layer and said first metal area forms a memory element." The examiner interprets this to mean that the 3rd metal (30), dielectric (25), and 1st metal (20) of the appellant's figure 1 together forms the memory element. Ryan (fig. 3) shows the exact same configuration because there is a third metal area (22), dielectric (16), and a first metal area (21). Based on the specific limitations of claim 1, the configuration of Ryan also inherently forms a memory element. It seems that the applicant is trying to read limitations into the claims or insert an intended use for capacitor, but the claims themselves do not recite any meaning other than the fact that the metal areas and the dielectric form a memory element. Because the structure and materials of the capacitor of Ryan are the same as the appellant's claimed invention, the capacitor of Ryan inherently forms a memory element.

(2) Ryan met all of the limitations of the appellant's claim 1 except the limitation of the second metal layer having an electrically conductive connection between said third metal area and said fourth metal area. The appellant's figure 1 shows that 4th metal area (50) has an electrical connection by the second metal layer to the 3rd metal area

(30). Ryan shows the 4th metal area (25) in figure 3 but lacks the electrical connection to the 3rd metal area (22). Therefore, Leung was cited to cure the deficiency by showing that 4th metal area (right side 134) forms an electrically conductive connection to the 3rd metal area (left side 134 over dielectric 130). In the rejection, it was stated that the benefits of the Leung configuration pertain to simplifying the connection process and forming the capacitor without disrupting the routing of the underlying metallization. One of ordinary skill in the art would further realize the configuration of Leung requires less materials and ultimately a greater packing density since less metallization and dielectric is needed to make the desired connections.

The appellant argues that Ryan cannot be combined with Leung because Leung is an on-chip analog capacitor. However, as stated above, analog and digital capacitors generally have the same structure; a dielectric layer formed between two conductive metal plates. Ryan, whether disclosing a digital or analog capacitor, still has the same capacitor configuration as Leung. As seen in Leung's figure 10, the capacitor portion has a first metal layer (128), a dielectric layer (130), and a second metal layer (134). Additionally, Leung also teaches a contact structure comprising shared second metal layer (134) and first metal layer (126). As seen from the figures, the second metal layer (134) is connected as the capacitor top electrode and as part of the interconnect (over 126). With such a configuration, the activation of the capacitor simultaneously provides a voltage to the interconnect or a voltage to the interconnect simultaneously activates the capacitor. One of ordinary skill in the art would apply this teaching to reduce the number of connections and vias to the interconnect and the capacitor of Ryan thus

reducing process steps and manufacturing costs. The applicant's arguments that the invention of Leung is beyond the scope of Ryan is also irrelevant. The purpose of combining references is to improve upon an invention. As stated in the rejection, Leung's invention provides additional benefits to Ryan's invention. Leung can be combined with Ryan because each invention pertains to a capacitor and a contact region. Therefore, the cited references show all of the elements of the claims and proper motivation for combining.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

ALLAN R. WILSON
PRIMARY EXAMINER

MEW
January 21, 2004

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